

Appl. No. 10/037,806  
Amdt. dated October 6, 2004  
Reply to Office action of August 9, 2004

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**REMARKS/ARGUMENTS**

Applicant acknowledges receipt of the Office action dated August 9, 2004. In that action, the Examiner: 1) rejected claims 12-28 as allegedly anticipated by Trainin (U.S. Patent Application Publication No. 2002/0144073); and 2) rejected claims 1, 3-11, 29-30, and 32-38 as allegedly unpatentable over Trainin in view of Roohparvar (U.S. Patent No. 6,504,768).

**I. CLAIM REJECTIONS**

**A. Claim 1**

Claim 1 stands rejected as allegedly obvious over Trainin in view of Roohparvar.

Trainin is directed to a method for memory heap management and buddy system management for service aware networks. (Trainin Title). While Trainin may disclose free memory block management by way of a linked list (see, e.g., Trainin Paragraph [0036]), Trainin makes no distinction between return of free memory blocks as between a software stream and a hardware device. Roohparvar is directed to redundancy selection in memory devices with concurrent read and write (Roohparvar Title), and is cited only for its concurrent aspects. It is noted, however, that Roohparvar deals with memory device level concurrent reads and writes, not management of free memory blocks, which could span several memory devices of the type disclosed in Roohparvar.

Claim 1, by contrast, specifically recites, "performing, **by a software stream**, heap memory operations on a first end of a linked list of free heap memory of a heap pile; and concurrently returning a return block of heap memory, **by a hardware device that used the return block of heap memory**, to the heap pile at a second end of the linked list of free heap memory." The Office Action dated August 9, 2004 takes the position that Trainin teaches differences in memory operations on a heap pile by a software stream and a hardware device citing Trainin's paragraph [0032]. This paragraph reads in full:

The present invention is described in the following exemplary embodiment with respect to a memory system that allocates memory blocks to tasks being executed using such memory. The present invention is also particularly well-suited for use in a SAN, where

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packet processors handle a plurality of process-flows, each with its own memory requirements. In SANs, process-flow processing is accomplished at wire speed, or the speed in which packets are moved through the network, which is paramount to the overall performance of the system.

(Trainin Paragraph [0032]). Applicant respectfully submits that the cited paragraph, or Trainin in general, fails to support the proposition for which it is cited. For this reason alone, claim 1 should be allowed.

Applicant further submits that Trainin taken with Roohparvar does not render obvious the limitations of claim 1. For example, Roohparvar does not supply the missing teaching regarding "returning a return block of heap memory, by a hardware device that used the return block of heap memory, to the heap pile at a second end of the linked list of free heap memory." Moreover, the concurrent reads and writes **to a memory device** of Roohparvar, taken with Trainin, fails to teach or suggest "performing ... heap memory operations on a first end of a linked list of free heap memory of a heap pile; and **concurrently** returning a return block of heap memory ... to the heap pile at a second end of the linked list of free heap memory." For these additional reasons, claim 1 should be allowed.

Based on the foregoing, Applicant respectfully submits that claim 1 is not rendered unpatentable by Trainin and Roohparvar, and should be allowed together with all claims that depend from claim 1 (claims 3-11).

#### **B. Claim 12**

Claim 12 stands rejected as allegedly anticipated by Trainin.

Trainin is directed to a method for memory heap management and buddy system management for service aware networks. (Trainin Title). While Trainin may disclose free memory block management by way of a linked list (see, e.g., Trainin Paragraph [0036]), Trainin fails to discuss any distinction regarding memory heap operations as between a software stream and a hardware device.

Claim 12, by contrast, specifically recites, "maintaining unused blocks of heap memory as a linked list, and wherein the unused blocks of the linked list comprise a first block at a beginning of the linked list, a second block pointed to the first block, and a third block at an end of the linked list; **removing, by a**

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software stream, the first block from the linked list, thus making the second block the beginning of the linked list; and returning a return block, by a hardware device that used the return block, to the linked list by placing the return block at the end of the linked list." The advantage of such a system is that the return and removal of memory blocks may take place simultaneously. (Specification Paragraph [0048]). The Office action dated August 9, 2004 takes the position that Trainin distinguishes between memory operations on a heap pile by a software stream and a hardware device citing Trainin's paragraph [0032]. This paragraph reads in full:

The present invention is described in the following exemplary embodiment with respect to a memory system that allocates memory blocks to tasks being executed using such memory. The present invention is also particularly well-suited for use in a SAN, where packet processors handle a plurality of process-flows, each with its own memory requirements. In SANs, process-flow processing is accomplished at wire speed, or the speed in which packets are moved through the network, which is paramount to the overall performance of the system.

(Trainin Paragraph [0032]). Applicant respectfully submits that the cited paragraph, or Trainin in general, fails to support the proposition for which it is cited.

Based on the foregoing, Applicant respectfully submits that claim 12 is not anticipated by Trainin, and should be allowed together with all claims that depend from claim 12 (claims 13-18).

#### C. Claim 19

Claim 19 stands rejected as allegedly anticipated by Trainin.

Trainin is directed to a method for memory heap management and buddy system management for service aware networks. (Trainin Title). While Trainin may disclose free memory block management by way of a linked list (see, e.g., Trainin Paragraph [0036]), Trainin fails to discuss any distinction regarding memory heap operations as between a software stream and a hardware device.

Claim 19, by contrast, specifically recites, "allowing a software thread to add and remove blocks of heap memory from a linked list of free blocks of heap

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memory in a last-in/first-out (LIFO) fashion **at a first end of the linked list**; and **allowing a hardware device** that uses blocks of heap memory to add the blocks of heap memory to the linked list of free blocks of heap memory **at a second end of the linked list.**" The advantage of such a system is that the return and removal of memory blocks may take place simultaneously. (Specification Paragraph [0048]). The Office Action dated August 9, 2004 takes the position that Trainin distinguishes between memory operations on a heap pile by a software stream and a hardware device citing Trainin's paragraph [0032]. Applicant respectfully submits that the cited paragraph, or Trainin in general, fails to support the proposition for which it is cited.

Based on the foregoing, Applicant respectfully submits that claim 19 is not anticipated by Trainin, and should be allowed together with all claims that depend from claim 19 (claims 20-28).

**D. Claim 29**

Claim 29 stands rejected as allegedly obvious over Trainin in view of Roohparvar.

Trainin is directed to a method for memory heap management and buddy system management for service aware networks. (Trainin Title). While Trainin may disclose free memory block management by way of a linked list (see, e.g., Trainin Paragraph [0036]), Trainin makes no distinction between return of free memory blocks as between a software stream and a hardware device. Roohparvar is directed to redundancy selection in memory devices with concurrent read and write (Roohparvar Title), and is cited only for its concurrent aspects. It is noted, however, that Roohparvar deals with memory device level concurrent reads and writes, not management of free memory blocks, which could span several memory devices of the type disclosed in Roohparvar.

Claim 29, by contrast, specifically recites, "wherein **the software stream executed on the microprocessor removes blocks of heap memory from a beginning of the heap pile; and simultaneously the hardware device returns blocks of heap memory used by the hardware device to an end of the heap pile.**" The Office action dated August 9, 2004 takes the position that Trainin

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teaches differences in memory operations on a heap pile by a software stream and a hardware device citing Trainin's paragraph [0032]. Applicant respectfully submits that the cited paragraph, or Trainin in general, fails to support the proposition for which it is cited. For this reason alone, claim 1 should be allowed.

Applicant further submits that Trainin taken with Roohparvar does not render obvious the limitations of claim 1. For example, Roohparvar does not supply the missing teaching regarding "returning a return block of heap memory, by a hardware device that used the return block of heap memory, to the heap pile at a second end of the linked list of free heap memory." Moreover, the concurrent reads and writes to a memory device of Roohparvar, taken with Trainin, fails to teach or suggest "the software stream executed on the microprocessor removes blocks of heap memory from a beginning of the heap pile; and simultaneously the hardware device returns blocks of heap memory used by the hardware device to an end of the heap pile." For these additional reasons, claim 29 should be allowed.

Based on the foregoing, Applicant respectfully submits that claim 29 is not rendered unpatentable by Trainin and Roohparvar, and should be allowed together with all claims that depend from claim 29 (claims 30, 32-38).

## **II. CONCLUSION**

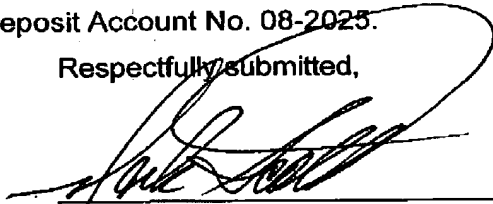
Applicant respectfully requests reconsideration and allowance of the pending claims. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned.

In the course of the foregoing discussions, Applicant may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

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Applicant respectfully requests reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,



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